Next Generation DSP Roadmap and related ESA activities

ADCSS09, ESTEC, the Netherlands

Session 3: New Development & Investigation Areas

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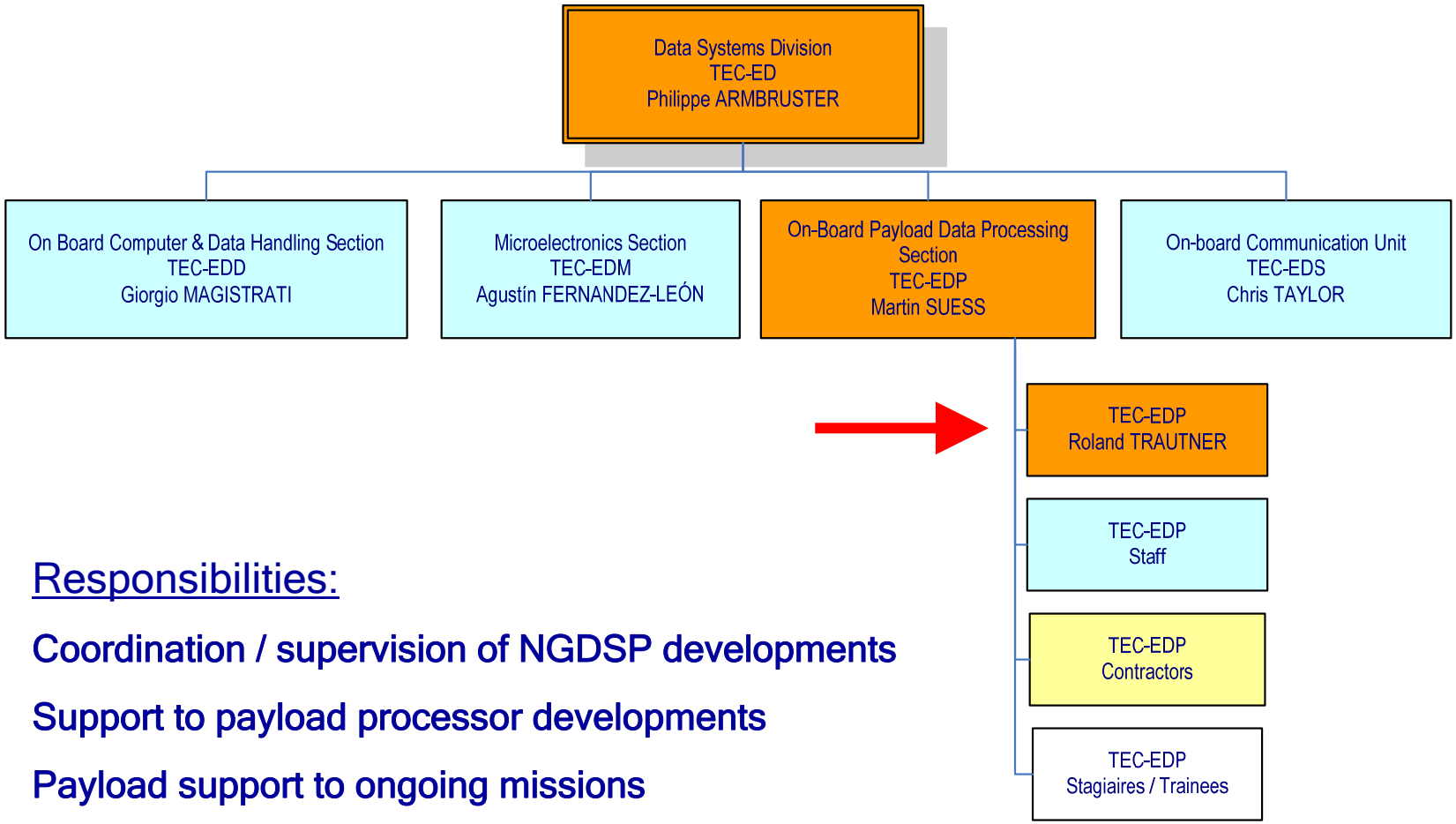
Onboard Payload Data Processing section (TEC-EDP)

ESA/ESTEC

TEC-ED: sections and association



Responsibilities:

Coordination / supervision of NGDSP developments

Support to payload processor developments

Payload support to ongoing missions

NGDSP: Current Situation & Future Mission Needs

CURRENT SITUATION

- Established space-qualified DSP (21020) is now outdated, much higher performance is needed
- For high processing power applications expensive ASIC / FPGA-based solutions are developed
- New developments urgently needed:

FUTURE MISSION EXAMPLES

- EUCLID / PLATO / SPICA (SRE) - up to few 100 MFLOPs (DSP)
- MTG IR sounder - I/F datarate ~2.2 Gbps peak, up to ~10 GFLOPS (DSP)
- High Res Wide Swath SAR - I/F datarate multi-Gbps, up to ~1 TOPS total (ASIC+DSP)

NGDSP: ADCSS07

ADCSS 2007 => NGDSP round table has been held with strong industrial participation

Report available at ADCSS07 website:

"Next Generation Processor for On-board Payload Data Processing Application ESA Round Table- Synthesis, TEC-EDP/2007.35/RT, October 2007"

Key NGDSP requirements have been established:

- 1 GFLOPS, rad-hardened design, EDAC, space specific / high speed IF
- ITAR free IP and processor, high quality SDE

NGDSP DEVELOPMENT OPTIONS

- 7 development options that could address the needs of the space community were identified
- presented, discussed and prioritized at ADCSS07 round table on NGDSP
- These are now addressed by various ESA activities

ADCSS07 - NGDSP Development Options 1/2

Option A: Hardening of COTS processors against radiation effects on computer board / software level

=> Board development based on commercial rad-tolerant processors, mitigation of radiation effects by a mix of HW and SW mechanisms (=> COTS uP presentation)

Option B: Hardening of COTS processors against radiation effects by using a space qualified ASIC process and transparent design modification

=> NGDSP implementation based on IP available from DSP manufacturers; successfully demonstrated previously with ADI 21020 DSP (=> ADI presentation)

Option C: Use of an available non-European rad-hard / rad-tolerant DSP

=> ESA is following Manufacturers (TI) efforts for improving radiation properties of these products (=> TI presentation)

ADCSS07 - NGDSP Development Options 2/2

Option D: Use of a multi-core DSP IP based processor

New processor architectures based on multiple cores, network on chip, integrated memories etc are interesting candidates for future processing elements

Option E: Use of a multi-core LEON3 IP based processor

=> Multi-core LEON is performant but not found suitable for DSP applications. => development in NGMPP (=> previous presentations)

Option F: Use of a combination of LEON and multi-core DSP

=> Use of LEON as a control processor for a specialized DSPcore, re-use of LEON heritage / knowhow / tools (=> ATMEL presentation)

Option G: Specific solutions based on ASIC / FPGA technology

=> Next Gen ASIC technology (65 nm) and re-programmable FPGAs addressed by dedicated TEC-E activities

Ongoing NGDSP-related ESA Activities - 1/4

Title

Next Generation DSP Tradeoff Study

Activity Summary

Evaluation of 3 modern high performance DSPs (design, complexity, adaptability, SDE) wrt. their suitability for space applications / flexibility for implementation as a space qualified ASIC on a space ASIC platform (65 nm), incl. downselection

Type / Contractor / Timeframe

TRP, AST-F, 09 2009 – 09 2010

Related NGDSP development options

Options (A, C) - evaluation of a QML-x COTS DSP / board level hardening

Option (B) – hardening of a COTS DSP on space ASIC platform and transparent design modification

Option (F) – Combination of LEON and DSP IP

Ongoing NGDSP-related ESA Activities -2/4

Title

Massively Parallel Processor Breadboarding Study

Activity Summary

FPGA based development of a scalable, massively parallel processor architecture based on LEON GPP (control processor), DSP & memory tiles, Network-on-Chip, standardized interfaces, off-chip network ports, and a set of benchmark software routines that allows comparison with 'conventional' DSPs

Type / Contractor / Timeframe

TRP, RECORE Systems, NL, 01 2009 - 01 2011

Related NGDSP development options

Option (D) - Use of a multi-core DSP IP based processor

Ongoing NGDSP-related ESA Activities -3/4

Title

High Performance COTS based Computer

Activity Summary

Phase I: Studies for a high performance DSP board based on COTS components and board level radiation mitigation techniques, supporting simulation

Phase II: Requirements and application case analysis, architectural and detailed design, hardware manufacturing of a EM-like breadboard, testing / evaluation / validation, benchmarking, demonstration of efficiency of design approach and achieved performance

Type / Contractor / Timeframe

GSTP, AST-F/CGS, 2009 (Phase I) and 2010-2011 (planned, Phase II)

Related NGDSP development options

Option (A,C) - hardening of a COTS DSP on computer board / SW level

Ongoing NGDSP-related ESA Activities -4/4

Title

High Performance Payload Digital Signal Processor

Activity Summary

Development of a high performance payload processor breadboard suitable for supporting SRE science mission candidates (PLATO, EUCLID, SPICA/SAFARI - 2016 … 2018 timeframe)

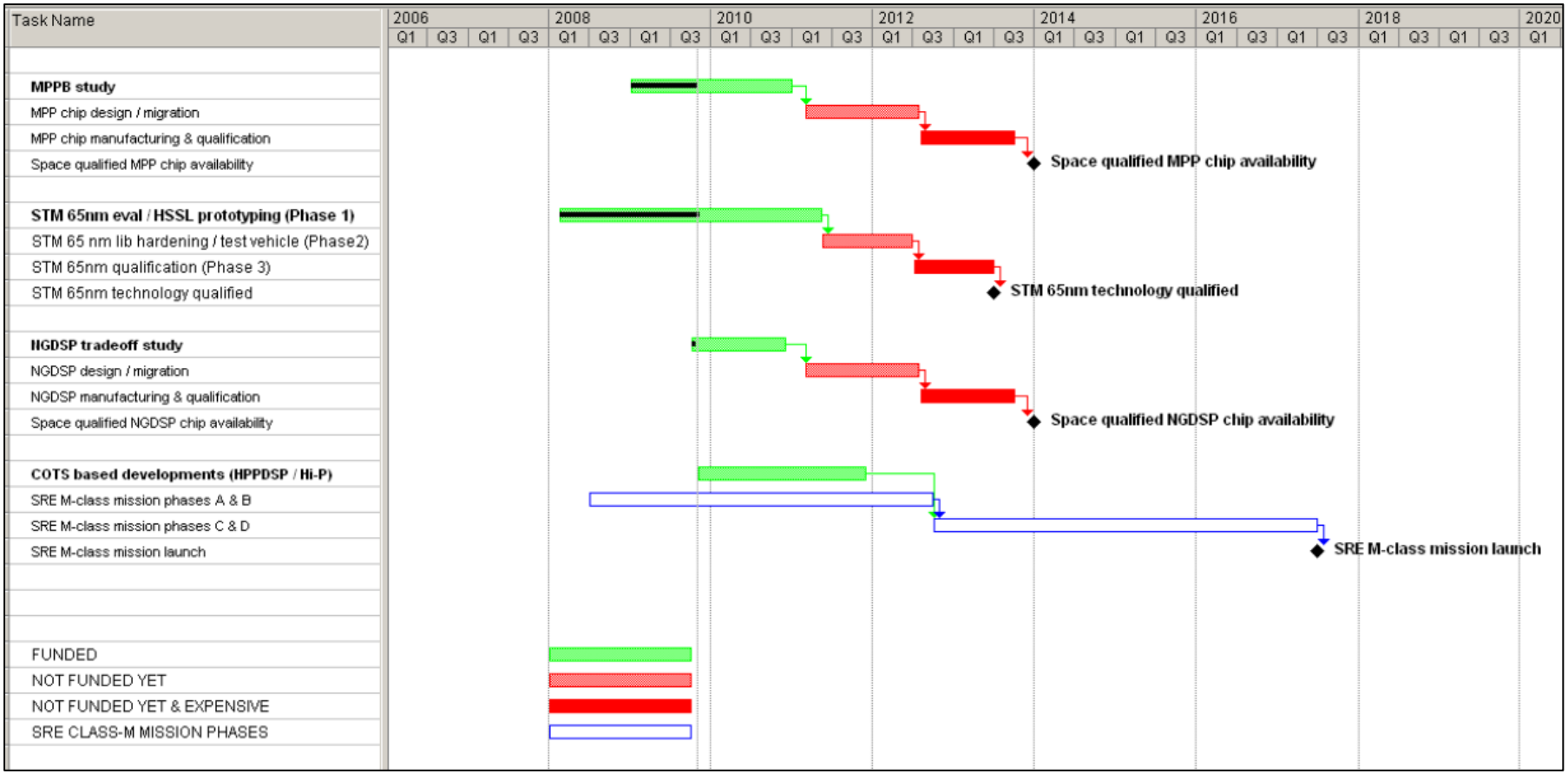
Type / Contractor / Timeframe

CTP (SRE-PA), Contractor TBD, end 2009 till 2011

Related NGDSP development options

Option (A,C) - hardening of a COTS DSP on computer board / SW level

Schedule Overview - NGDSP related activities



Supportive Elements for NGDSP development

At ADCSS07 the need for a NGDSP benchmark was identified

ESA has defined such a benchmark:

"Next Generation Space Digital Signal Processor Software Benchmark", TEC-EDP 2008/018/RT, Issue 1 available since December 2008

Available via email request: *SpaceDSP.benchmark@esa.int*

This benchmark is applied in the following activities:

- NGDSP tradeoff study (COTS DSPs)
- Massively Parallel Processor Breadboard (DSP / NoC)
- HPPDSP (board-level hardened COTS DSPs)
- Hi-X CoCs (board-level hardened COTS processors including PPC)

Further NGDSP development support is provided via internal TEC-EDP activities

NGDSP-related ESA Activities: Summary

New, more powerful processing elements needed

ADCSS07 round table has identified possibilities and defined key requirements

7 development options

ESA is following recommendations and ongoing developments address the options

Needs for upcoming missions are addressed with dedicated developments

Supportive activities

NGDSP benchmark defined and available, minor questions addressed in-house

Schedule & Roadmap

Next 1-2 year activities defined and currently executed

Ongoing NGDSP developments will allow to downselect the available options

Plan for following phases in place => funding needs to be secured